Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

<u>REMARKS</u>

Present Status of the Application

The Office Action rejected all presently-pending claims 1-20. Specifically, the Office Action rejected claims 1-18 under 35 U.S.C. 102(b), as being anticipated by Yu et al. (U.S. Pat. 6,571,485, "Yu et al." hereinafter). The Office Action also rejected claims 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Yu et al. in view of Fahey et al. (U.S. Pat. 5,447,884, "Fahey et al." hereinafter).

In response thereto, Applicant has cancelled claim 9 and has amended claims 1 and 10 to more clearly define the present invention. After entry of the foregoing amendments, claims 1-8, 10-18 and 20 remain pending in the present invention, and reconsideration of those claims is respectfully requested.

Claim Rejections under 35 U.S.C. 102(b)

The Office Action rejected claims 1-18 under 35 U.S.C. 102(b) as being anticipated by Yu et al. In response thereto, Applicant has amended independent claims 1 and 10 and hereby otherwise traverse the 102(b) rejection of claims 1-18 because Yu et al. does not teach each and every element recited in these claims.

The present invention is related to a stress relieving method as amended claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:

Page 5 of 9

and

Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that at least no circuits are formed on the dielectric layer within the first area;

forming a plurality of first openings in the dielectric layer within the first area; and

forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings, and the first material layer is a high stress dielectric layer. (Emphasis added)

The office action stated that Yu et al. disclosed all the claimed subject matter except the feature that the first material layer is a high stress dielectric layer. To better distinguish the prior art and the present invention, Applicant has amended claim 1 by incorporating said limitation originally recited in claim 19 into claim 1, and thereby Yu et al. no longer teaches every element of claim 1. Thus, claim 1 should be allowable.

In addition, Applicant has amended claim 10 as follows,

Claim 10. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area, wherein there is no opening formed in the dielectric layer within the first area;

forming a first material layer over the wafer to cover the dielectric layer;

forming a plurality of first openings in the first material layer within the first area.

The Examiner asserted that the first material layer in claim 10 of the present

Page 6 of 9

Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

application denotes the metal layer 204 in Fig. 2 of Yu et al., and the teaching in column 1, lines 44-47 of Yu et al. discloses the technical feature of the Applicant's invention, suggesting a portion of the first material layer with the first area is removed to form a plurality of first openings. However, Applicant respectfully disagrees said assertion, for the description in column 1, lines 44-47 of Yu et al. merely teaches a portion of the metal layer 204 that is formed out of the via hole and the trench is removed through a chemical mechanical polishing (CMP) process, such that the metal layer 204 formed in the via hole is kept. Moreover, since the trench 207 is already formed in the dielectric layer 205 in Yu et al., the trench still exists after the CMP process is performed. Nevertheless, in Applicant's amended claim 10, there is no opening formed in the dielectric layer within the first area.

In view of the foregoing or other reasons, Applicant respectfully submits Yu et al. fails to teach or suggest every element recited in claim 1 or in claim 10. Therefore, after entry of the amendments, Applicant respectfully submits that independent claims 1 and 10 patently defines over the prior art reference, and should be allowed. Since independent claims 1 and 10 should be allowed over the prior art of record, its dependent claims 2-8 and 11-18, 20 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claims 1 and 10. In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

Claim Rejections under 35 U.S.C. 103(a)

The Office Action rejected claims 19 and 20 under 35 U.S.C. 103(a), as being unpatentable over Yu et al. in view of Fahey et al. Applicant respectfully traverses the

Page 7 of 9

Customer No.: 31561
Docket No.: 12336-US-PA
Application No.: 10/710,662

rejections for at least the reasons set forth below.

In response thereto, Applicant has incorporated the limitation indicated in claim 19 into claim 1 and accordingly cancelled claim 19. After entry of the aforesaid amendments, Applicant submits that, as discussed above, Yu et al. fails to teach or suggest each and every element of claim 10 on which claim 20 originally depend.

Besides, the office action states that the oxide filler 60 in Fig. 5 of Fahey et al. refers to the first material layer which is, after entry of amendments to claim 1, a high stress dielectric layer in the Applicant's invention. However, referring to Fig. 5 of Fahey et al., the oxide filler 60 is filled in the trench in the shallow trench isolation, while the high stress dielectric layer of the present application is formed over the metallic interconnects.

Based on the above, independent claim 10 is patentable over *Yu et al. and Fahey et al.*For at least the same reasons, its dependent claim 20 is also be patentable as a matter of law.

RECEIVED
CENTRAL FAX CENTER

FEB 15 2007

Customer No.: 31561 Docket No.: 12336-US-PA Application No.: 10/710,662

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-8, 10-18, and 20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date:

Ach. 16, 2007

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office 7th Floor-1, No. 100 Roosevelt Road, Section 2 Taipei, 100 Taiwan

Tel: 011-886-2-2369-2800 Fax: 011-886-2-2369-7233

Email: belinda@jcipgroup.com.tw Usa@jcipgroup.com.tw